Forum of Electromagnetic Research Methods and Application Technologies (FERMAT)

On-Chip, Efficient and Small Antenna Array for Millimeter-Wave Applications

H. Dinis, M. Zamith, J. Fernandes, J. Magalhães, P. M. Mendes
Contact: P. M. Mendes (pmendes@dei.uminho.pt)

MEMS-UMinho Research Unit, University of Minho,
Campus de Azurém, 4800-058 Guimarães, Portugal

Abstract— The high path losses experienced by wireless applications at millimeter wavelengths may be mitigated using high gain antennas. The intrinsic small wavelengths makes very attractive to develop solutions with on-chip integrated antennas. However, due to silicon high losses, on-chip antenna elements on RFCMOS technology have reduced efficiency. This paper proposes a solution to obtain an on-chip integrated antenna array based on 3D efficient antenna elements. A 4 element antenna was designed to operate at 57.5 GHz central frequency, with maximum gain of 5.8 dB, and maximum expected efficiency of 45%.

Keywords—integrated antenna, on-chip antenna, antenna array, 60 GHz.

I. Antenna Fabrication & Integration

Fig. 1 shows the proposed antenna integration concept. The four antenna elements are obtained using 3D self-folding methodology. After obtaining the antenna array on top of a silicon wafer, the integration with the remaining system may be obtained using wafer level chip scale packaging methodologies, multi-chip methodologies, or by using a post-processing module applied to the RFCMOS wafer [1].

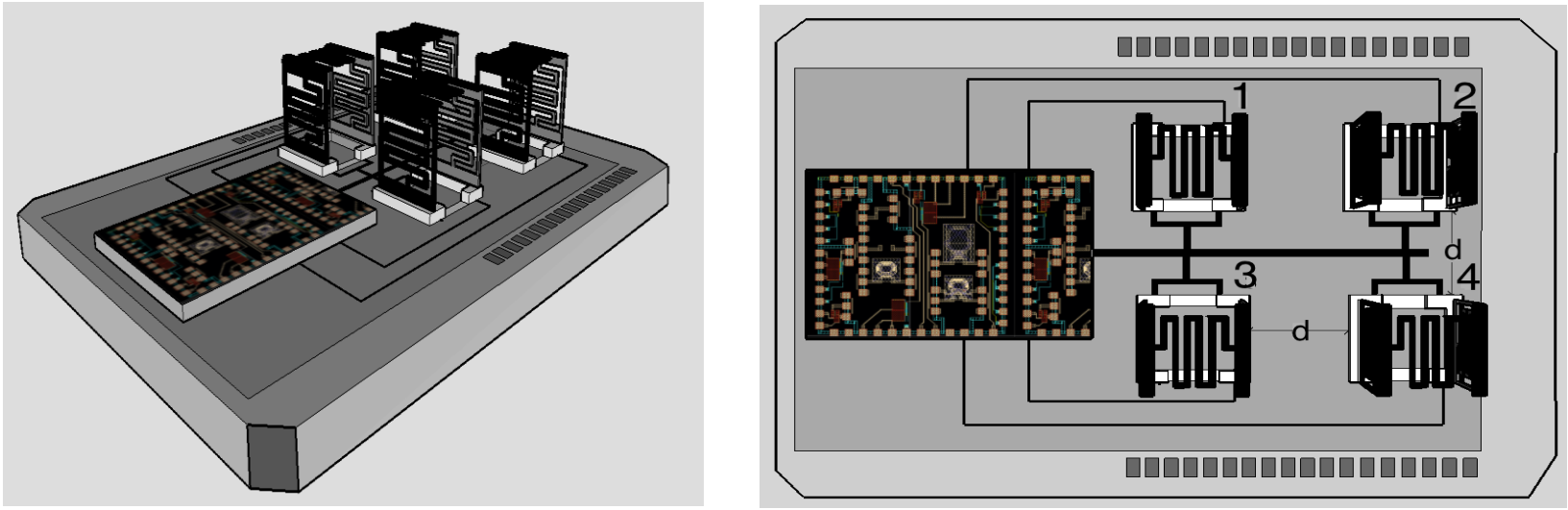


Fig. 1 - On-Chip Antenna Array Concept

In Fig. 2, it's possible to see all the steps of the self-folding process.

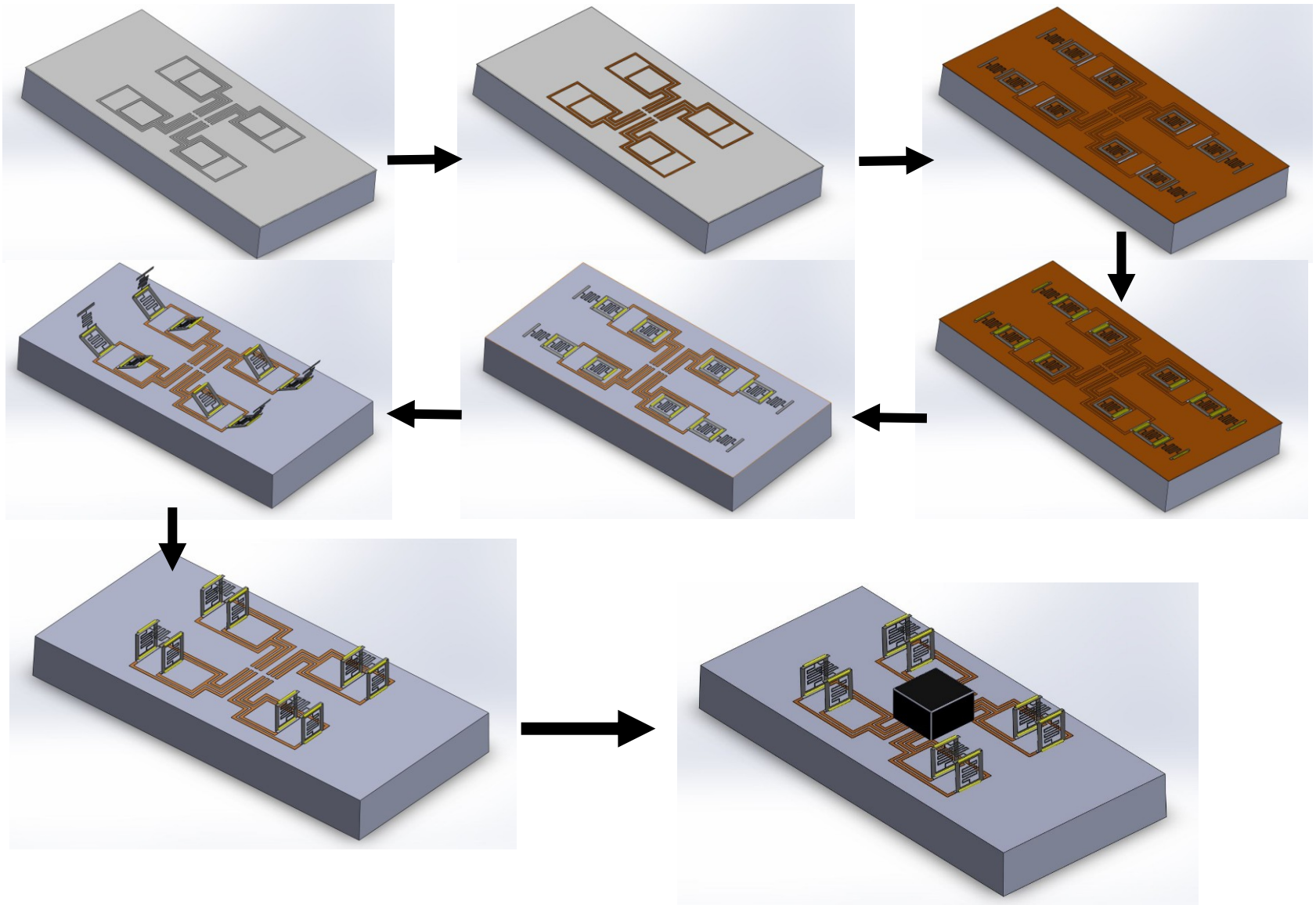


Fig. 2 – On-Wafer Self-folding Process Steps

II. Antenna Modeling

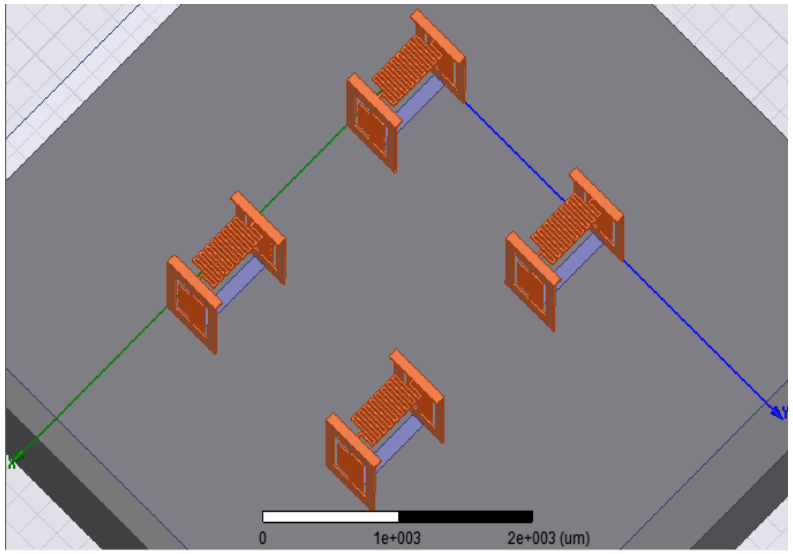


Fig. 3 – HFSS 3D Modeling

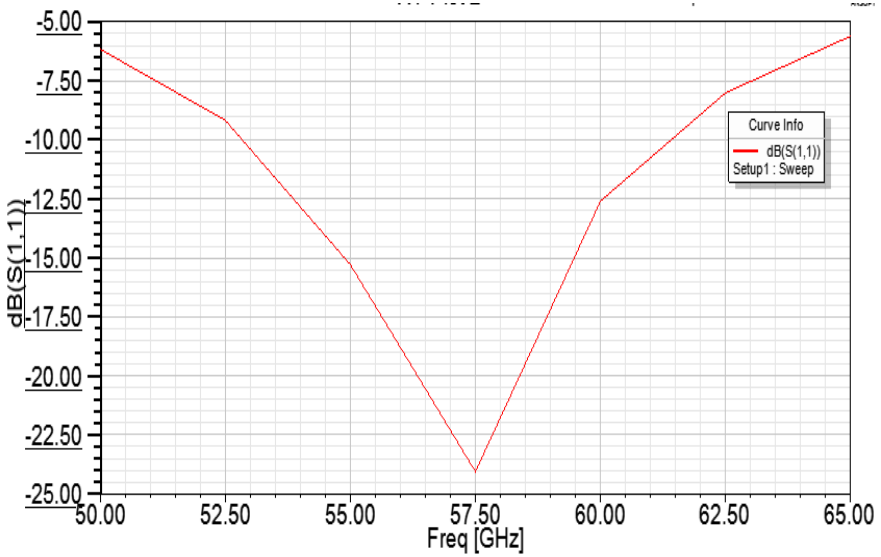
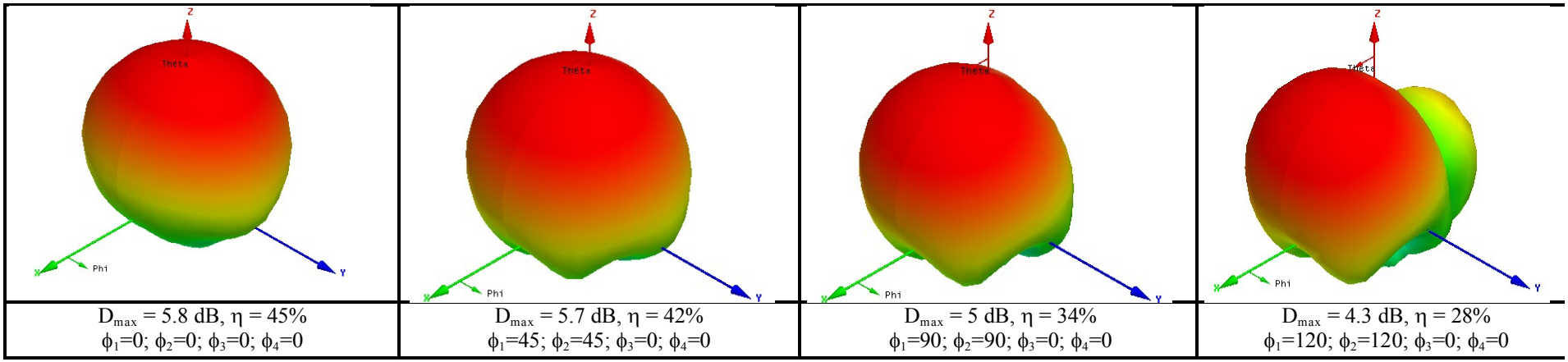


Fig. 4 – Operating Frequency and Bandwidth



D_{max} = 5.8 dB, η = 45% ϕ_1=0; ϕ_2=0; ϕ_3=0; ϕ_4=0	D_{max} = 5.7 dB, η = 42% ϕ_1=45; ϕ_2=45; ϕ_3=0; ϕ_4=0	D_{max} = 5 dB, η = 34% ϕ_1=90; ϕ_2=90; ϕ_3=0; ϕ_4=0	D_{max} = 4.3 dB, η = 28% ϕ_1=120; ϕ_2=120; ϕ_3=0; ϕ_4=0

Fig. 5 – Antenna Gain and Efficiency

Fig. 3 shows the HFSS antenna model. It shows the four-antenna element, with a close-up to one single antenna. The antennas are placed on top of a silicon wafer, with electrical permitivitty, ε_r=4.25, and loss tangent, tanδ=0.15 [2]. It was assumed that the wafer bottom was grounded and no isolation layer, like SiO2 was placed on top of the wafer, between antennas and silicon wafer.

In Fig. 4 the antenna operating central frequency and bandwidth is shown. Using the antenna array model from Fig. 3, the results shown in Fig. 5 were obtained for a distance between antennas of d = 1.15 mm Since we have four antennas, the radiation pattern may be controlled using the phase shifts. Also from Fig. 5, we can see that the maximum efficiency was η = 45% and max gain was G = 5.8 dB. The gain and efficiency changes as we change the radiation pattern. The values shown in table 1 may not seem very high, but when compared with values from [3], we may conclude that this new approach is very competitive, since it gives almost the same values without the need of extra room required by the artificial materials. Moreover, this new approach does not require any complex antenna design methodology.

III. Proposed Antenna Characterization Setup

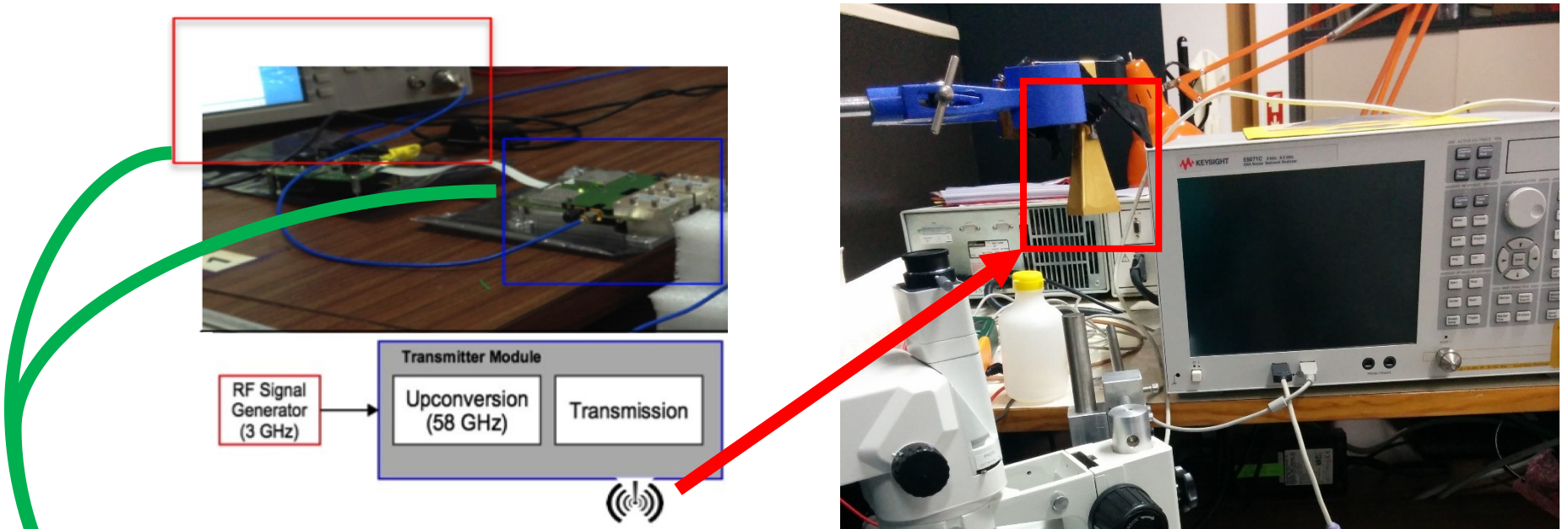


Fig. 6 - Siversima MMW module based setup

Fig. 7 - RFCMOS receiving circuit [2] and antenna array on top of Si die

IV. Conclusions

In this work we propose the integration of 3D antennas on top of a silicon wafer. A solution was proposed towards the development of fully integrated RFCMOS transceivers at millimetre-wave band, with improved efficiency.

Acknowledgement

Work supported by Portuguese Foundation for Science and Technology (SFRH/BD/63737/2009, and PTDC/ EEI-TEL/ 2881/2012, Programa Operacional Temático Fatores de Competitividade-COMPETE, and Fundo Comunitário Europeu-FEDER).

References

[1] S. Pandey, E. Gultepe, D. H. Gracias, “Origami inspired self-assembly of patterned and reconfigurable particles.,” J. Vis. Exp., no. 72, p. e50022, 2013.

[2] F. Guttierrez , T. S. Rappaport and J. Murdock "Millimeter-wave CMOS antennas and RFIC parameter extraction for vehicular applications", Proc. IEEE Vehicular Technology Conf., 2010

[3] A. Barakat, A. Allam, H. Elsadek, “Small Size 60 GHz CMOS Antenna-on-Chip: Gain and Efficiency enhancement using asymmetric Artificial Magnetic Conductor,” in 44st European Microwave Conference (EuMC), Rome, Italy, 5-10 October, 2014.

[4] - M. Zamith, J. Magalhães, P. Anacleto, P. M. Mendes, “60 GHz On-Chip Antenna Array with Efficiency Improvement Using 3D Microfabrication Technology”, The 9th European Conference on Antennas and Propagation, Lisbon, Portugal, on 12-17 APRIL 2015.